REMARKS/ARGUMENTS

In the Office Action mailed May 1, 2007, the Examiner designated the Amendment filed February 12, 2007[1] as non-responsive for failing to specifically point out how the language of the new claims patentably distinguishes them from the references, and in particular, requested Applicant to draw a distinction between the new claims and the Hasbun reference. In the May 1, 2007 Office Action, the Examiner indicated the distinction over Hasbun is considered "vital" due to "overlapping subject matter" between the previously-pending claim 31 and the then-new claim 65. Claim 31 had been canceled in the Feb. 12 amendment, but was previously rejected as anticipated by Hasbun.

It is respectfully submitted that the remarks in this amendment specifically points out patentable distinctions between the pending claims and the references, including the Hasbun reference. In addition, the previously submitted claims have been carefully reviewed and amendments to the claims, as well as new claims 75-77, have been added for greater clarity. Entry of this amendment, and further examination and reconsideration of the application, are respectfully requested.

Claim 31 and Claim 65 Differences

It is submitted that there are clear differences between canceled claim 31 and claim 65. As noted in the May 1 Office Action, claim 31 and claim 65 both recite a feature of detecting a write operation to a memory including a re-programmable non-volatile memory. It is there that the similarity ends.

The canceled claim 31, after reciting the feature of detecting the write operation, then recites determining a caching location that identifies an area of dynamic memory to which data can be cached, and writing the data to the caching location instead of writing the data to the re-programmable non-volatile memory.

[1] The February 12, 2007 amendment was filed in response to the Office Action mailed August 10, 2006.

Claim 65, after reciting the feature of detecting the write operation, contains no mention of caching location nor of dynamic memory, but instead then recites performing a first write operation of data to the non-volatile memory if an address of the write operation indicates a first address area of the non-volatile memory, and performing a second write operation of data to the non-volatile memory if the address of the write operation indicates a second address area of the non-volatile memory, according to a write operation speed that is different from the first write operation speed.

Thus, claim 65 does not recite the claim 31 elements of a "caching location" in "dynamic memory" to which data is written instead of the non-volatile memory, and it is asserted that there is limited overlapping scope between the claims. With these distinctions in mind, Applicant will explain how claim 65 (and all the other pending claims) are patentably distinct over the cited references.

Hasbun

In the prior Office Action of August 10, 2006, the Examiner asserted that Hasbun taught all claim elements of since-canceled claim 31.[2] Hasbun relates to using flash memory as main memory in a computer, and writes data in main memory to a cache buffer or to a holding buffer depending on the available capacity of each (see Hasbun at col. 2, lines 19-38). Hasbun contains no mention at all of controlling the speed of write operations; it is apparent that the writing speed is fixed. In contrast, all of the pending independent claims recite controlling the speed of write operations in accordance with the write address. Claim 65 is illustrative:

> 65. A memory access method comprising:
>
> detecting a write operation to a memory including a re-programmable non-volatile memory;

[2] The Examiner also asserted that Hasbun anticipates claims 32-37 and 40-50, all of which have previously been canceled with the response of February 12, 2007.

if an address of said write operation from a processor logic indicates a first address area of said non-volatile memory, then performing a first write operation of data to said non-volatile memory; and

if said address of said write operation from a processor logic indicates a second address area of said non-volatile memory, then performing a second write operation of data to said non-volatile memory according to a write operation speed that is different from the first write operation speed.

The other independent claims (67, 73, 76) contain similar limitations regarding speed of the write operations, which are not taught or suggested by Hasbun. For example, newly presented claim 76 recites:

76. A data processing unit comprising:

memory that includes re-programmable non-volatile memory into which data is written; and

control logic configured for detecting a write operation to the memory and for performing the write operation to a first address area of the non-volatile memory at a first write operation speed if an address of the write operation indicates a first memory area of the memory and for performing the write operation to a second address area of the non-volatile memory at a second write operation speed if an address of the write operation indicates a second memory area of the memory, wherein the first write operation speed is different from the second write operation speed. (emphasis added)

It is apparent that the writing speed of Hasbun is fixed. In contrast, the pending claims recite writing operations such that "if said address of said write operation ... indicates a second address area of said non-volatile memory, then performing a second write operation of data to said non-volatile memory according to a write operation speed that is different from the

first write operation speed (from claim 65, emphasis added). Therefore, all the independent claims, and the claims dependent therefrom, are patentably distinct over Hasbun.

Tobita

In the prior Office Action of August 10, 2006, the Examiner asserted that Tobita anticipated the since-canceled claims 51-55. As noted in the prior response of February 12, 2007, Tobita describes a controller in which the writing speed is fixed according to the flash memory module. All of the pending independent claims (65, 67, 73, 76) recite performing write operations at different speeds in accordance with the write address. Tobita suffers from the same deficiencies as Hasbun and therefore all of the claims are patentably distinct over Tobita. Therefore, all the independent claims and the claims dependent therefrom are patentably distinct over Tobita.

Hasbun + Agarwal

In the prior Office Action of August 10, 2006, the Examiner asserted that Hasbun in combination with Agarwal rendered obvious the since-canceled claims 38-39. As noted above, Hasbun does not contain any recitation of controlling the speed of write operations. Agarwal does nothing to remedy that situation. The Examiner cited Agarwal for describing the step of identifying one or more memory locations based on contents of data. Because all of the pending independent claims (65, 67, 73, 76) recite controlling the speed of write operations, and because Agarwal does not make up for the deficiencies of Hasbun, it is asserted that the pending claims 65-77 are patenably distinct over the proposed combination of Hasbun and Agarwal.

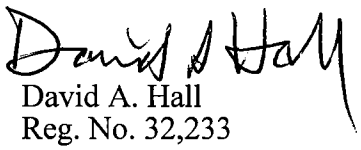
Remaining References

The remaining references of record have been reviewed and do not describe the invention of claims 65-77. The remaining references do not make up for the deficiencies of Hasbun, Tobita, and Agarwal. It is asserted that the limitations in the pending claims 65-77 are not contained in the references nor suggested by the specifications of the references.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

Respectfully submitted,



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